A SINGLE-CHIP PHS FRONT-END MMIC WITH A TRUE SINGLE +3V VOLTAGE SUPPLY

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ABSTRACT

A small single-chip PHS RF front-end GaAs MMIC operating with single +3V supply voltage has been developed. This MMIC integrates transmitter power-amplifier, receiver LNA, switchable attenuator, RX/TX switches, and control logic in a single-chip. Unlike conventional GaAs MESFET technology, the new power GaAs MESFET incorporated in this chip does not require negative voltage gate bias, and as a result, the MMIC can be operated by a true single-supply voltage without internal or external negative voltage generator.

INTRODUCTION

Like many other mobile telecommunication systems, there has been a strong trend towards ultra miniature portable handsets for the 1.9GHz personal handy phone system (PHS). For this miniaturization in handsets to be realized, single-chip solutions for RF front-end function with single-supply voltage operation are especially important. Because the conventional GaAs power MESFETs require both negative and positive supply voltages, the single-chip single supply-voltage RF front-end MMICs developed to date integrate an internal negative voltage generator (NVG) on the same chip [1]-[4]. However incorporation of NVG creates serious problems related to the amount of IC die area required for the design. In some cases one-fourth of the chip die area is required for the NVG. Besides the valuable IC die realestate that is wasted by the NVG circuitry, the NVG operation causes additional power consumption and tends to generate spurious noise radiated from its switching operation that can seriously impair the total performance of the chip. The single-chip PHS front-end MMIC described in this paper operates with a true single bias +3V supply and avoids the need for the internal as well as external NVG circuitry.

BASIC DEVICES AND FABRICATION PROCESS

The MMIC design was carried out based on a newly developed GaAs process, the Murata Semiconductor Standard Process-3B (MSSP-3B). This standard process uses new MESFET technology with buried gate structure and enables the fabrication of depletion/enhancement MESFETs of different pinch-off voltages, that are controllable between -2.0 and +0.8V. As a result, power, low noise, and logic circuits can be integrated on a single IC die. Because of the high Schottky barrier height of this unique gate structure, the power FETs can be operated by single +3V supply voltage (Fig. 1). The output characteristics in Fig. 1 is obtained with 1.4 mm FET and shows a high efficiency performance under the single +3V condition.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

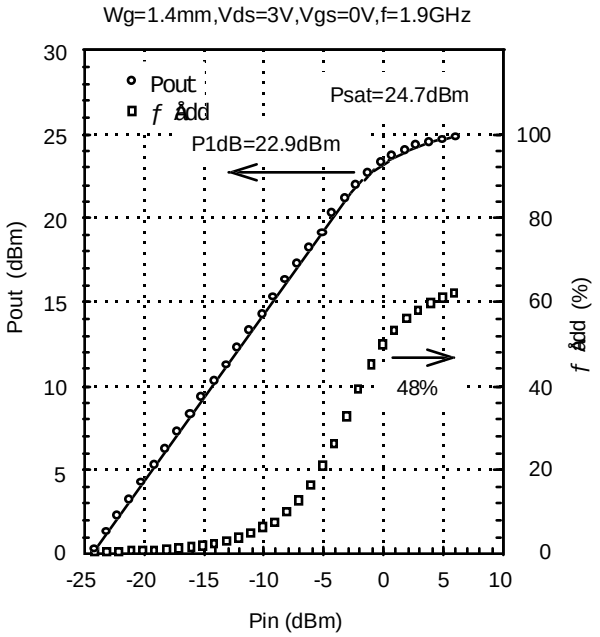

Fig.1, Output power and power added efficiency

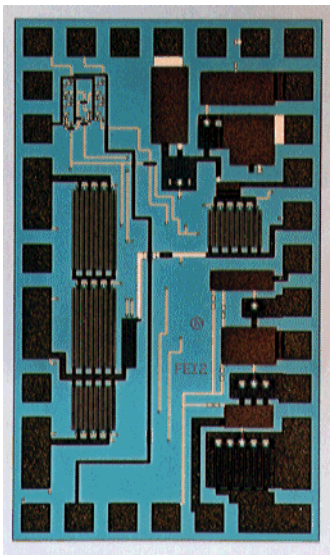

Fig. 3, MMIC photograph

OUTLINE OF MMIC

This front-end MMIC incorporates PA, LNA, switchable attenuator for high field reception, RX/TX switches, and control logic on the same chip. The schematic block diagram of the MMIC is shown in Fig. 2. Figure 3 shows the photograph of the fabricated MMIC. The chip size is as small as 1.1mm x 1.9mm, because the internal NVG is not required. The design and performance of each circuit block are as described below. The IC package used for this MMIC is a thin SSOP-24 plastic mold package. All characteristics shown below are measured on an evaluation printed circuit board (PCB) on which the SSOP-24 packaged MMIC is mounted.

SWITCHES AND ATTENUATOR

The antenna switch on the RX side as well as the switchable attenuator respectively use two switch FETs in series, to ensure enough isolation from the TX side. Figure 4 shows the dependence of on-resistance (R_{on}) and off-capacitance (C_{off}) on the gate width (W_g) of the switch FETs. The optimized gate widths have been determined according to this diagram. The

Fig. 2, Circuit block diagram

switchable attenuator is constructed by combining a narrow W_g FET and a series connected resistor to generate the required attenuation level of -20dB. The small-signal characteristics of the RX/TX switches and attenuator are shown in Table 1. The obtained insertion losses (IL) is as small as 0.65 dB and 0.65 dB respectively for the RX and the TX switch. This small insertion losses derive from the inherently low on-resistance of these new FETs. On the other hand, to enhance the isolation between RX and TX, a SPST switch has been incorporated just after the LNA output port. The overall RX-TX isolation including the effect of this SPST switch results in a large value as 33 dB. These excellent results ensure the switch performance which is required for the PHS front-end application.

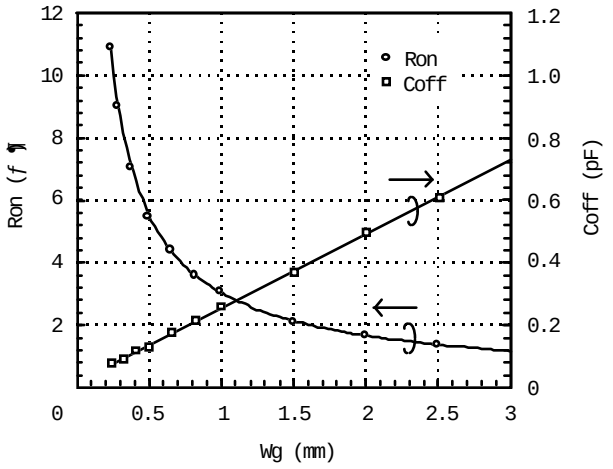

Fig. 4, R_{on} and C_{off} vs. total gate width

LOW NOISE AMPLIFIER

Figure 5 shows circuit schematic for the LNA. For the purpose of chip size reduction, the matching circuits are removed from the chip and provided on the PCB on which the MMIC is mounted. The FET switch connected in series to the drain terminal serves as the stand-by mode switch. The capacitor shunting this switch FET realizes the RF-short and prevents the output loss. The measured noise and gain characteristics are shown in Fig. 6, and are 1.8 dB and 13.5 dB respectively at 1.9GHz. The current consumption is 3mA. Thus, this LNA has realized low noise-figure, low current consumption, and high gain characteristics.

POWER AMPLIFIER

Figure 7 shows equivalent circuit for the PA, that consists of a 3 stage amplifier. The power FET in the 3rd output stage has the gate width of 1.4 mm. The input/output matching circuits as well as the interstage matching circuits are provided on the external PCB to minimize the chip size. The output power (P_{out}), operating current (I_{dd}), and adjacent channel power (ACP) vs. input power characteristics are shown in Fig. 8, where P1dB is

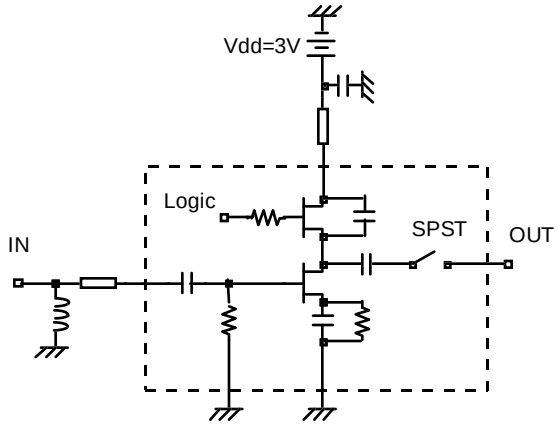

Fig. 5, LNA circuit schematic

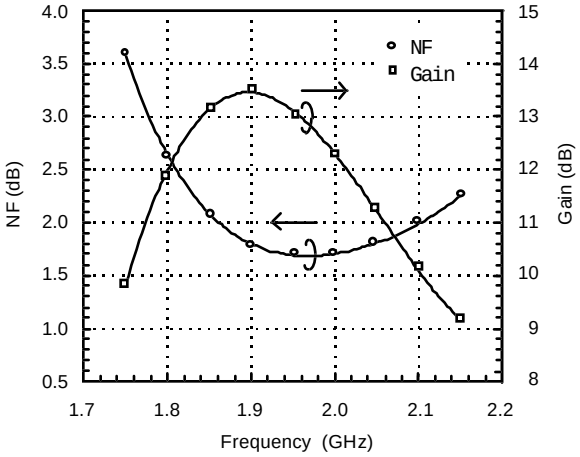

Fig. 6, Gain and NF of the LNA

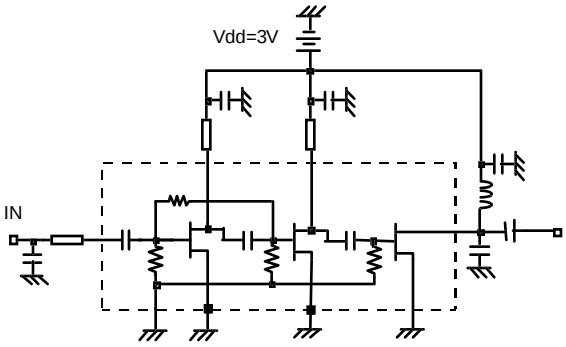

Fig. 7, PA circuit diagram

21 dBm and gain at P1dB (G1dB) is 36 dB respectively. The current consumption is as small as 145mA at the P1dB point of 21dBm. The ACP at P1dB is -58dBc. This small current consumption will be very effective for extending battery life.

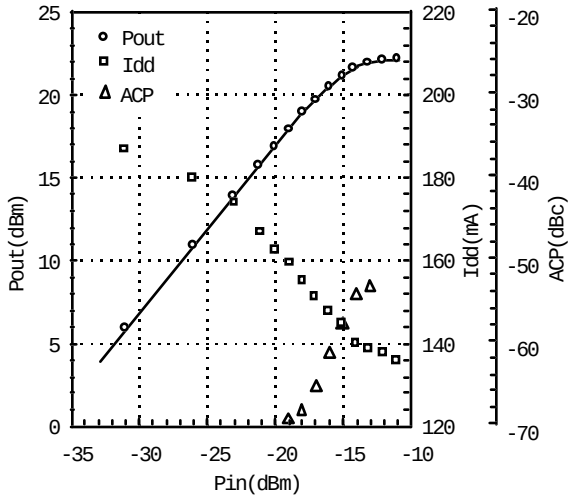

Fig. 8, P_{out}, I_{dd}, ACP vs. input power

CONTROL LOGIC

The circuit diagram is shown in Fig. 9. The DCFL construction using enhancement/ depletion FETs reduces the circuit complexity and, as a result, the occupied area. The E-FET level-shifters adjust the threshold level (V_{th}) to be at 1.5V so that it can be operated for the input low/high levels of 0V/3V. This logic circuit controls RX/TX switches, attenuator switching, and on/off of the LNA.

Overall characteristics are summarized in Table 1.

Table1, MMIC performance

Parameter	Characteristics
SW TX Insertion Loss	0.65 dB
SW RX Insertion Loss	0.65 dB
Total isolation from TX to SPST out	33 dB
Attenuation	-21 dB
LNA Noise Figure	1.8 dB
LNA Gain	13.5 dB
LNA Current Consumption	3 mA
PA P1dB	21 dBm
PA G1dB	36 dB
PA ACP @600KHz	-58 dBc
PA Current Consumption	145 mA
Logic Vth	1.5 V

Test Condition : V_{dd}=3.0V, f=1.9GHz

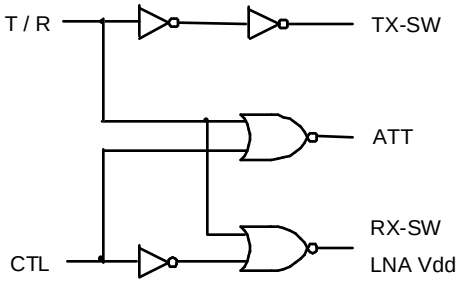

Fig.9, Logic circuit diagram

CONCLUSIONS

A single-chip 1.9GHz PHS front-end MMIC with a true single +3V supply operation has been presented. It achieves excellent performance and especially low current consumption by utilizing a new Murata GaAs MESFET technology. Furthermore, because of no internal negative voltage generator, the chip size can be much smaller than those obtained by conventional technology, application of the chip becomes much simpler for the RF designer, and finally the total cost of the RF front-end circuit can be greatly reduced.

ACKNOWLEDGMENT

The authors would like to thank Mr. H.Ariyoshi for his encouragement and support.

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